OIPE
MAY 22 2006
PATENT & TRADEMARK OFFICE

Fig. 1A
PRIOR ART

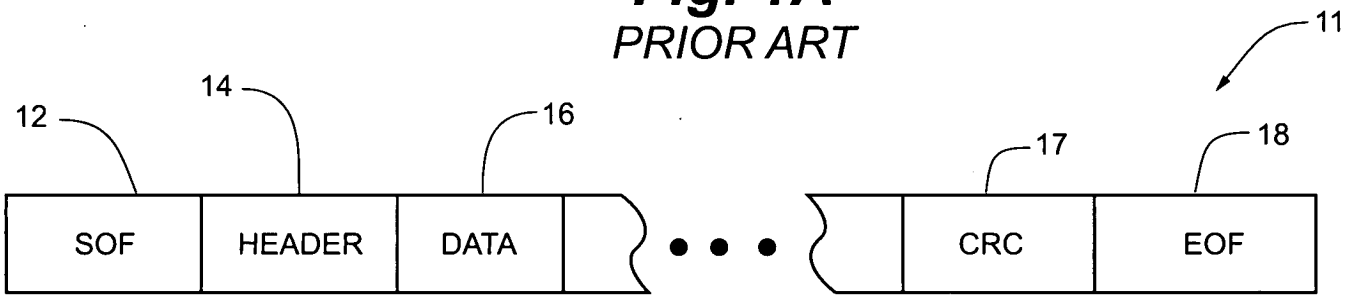
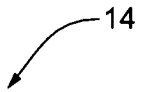


Fig. 1B
PRIOR ART



ROUTING CONTROL (R_CTRL)	DESTINATION ID (D_ID)	
CLASS SPECIFIC CONTROL (CS_CTL)	SOURCE ID (S_ID)	
DATA STRUCTURE TYPE (TYPE)	FRAME CONTROL (F_CTL)	
SEQUENCE ID (SEQ_ID)	DATA FIELD CONTROL (DF_CTL)	SEQUENCE COUNT (SEQ_CNT)
ORIGINATOR ID (OX_ID)		RESPONDER ID (RX_ID)
PARAMETER OR RELATIVE OFFSET		

Fig. 2
PRIOR ART

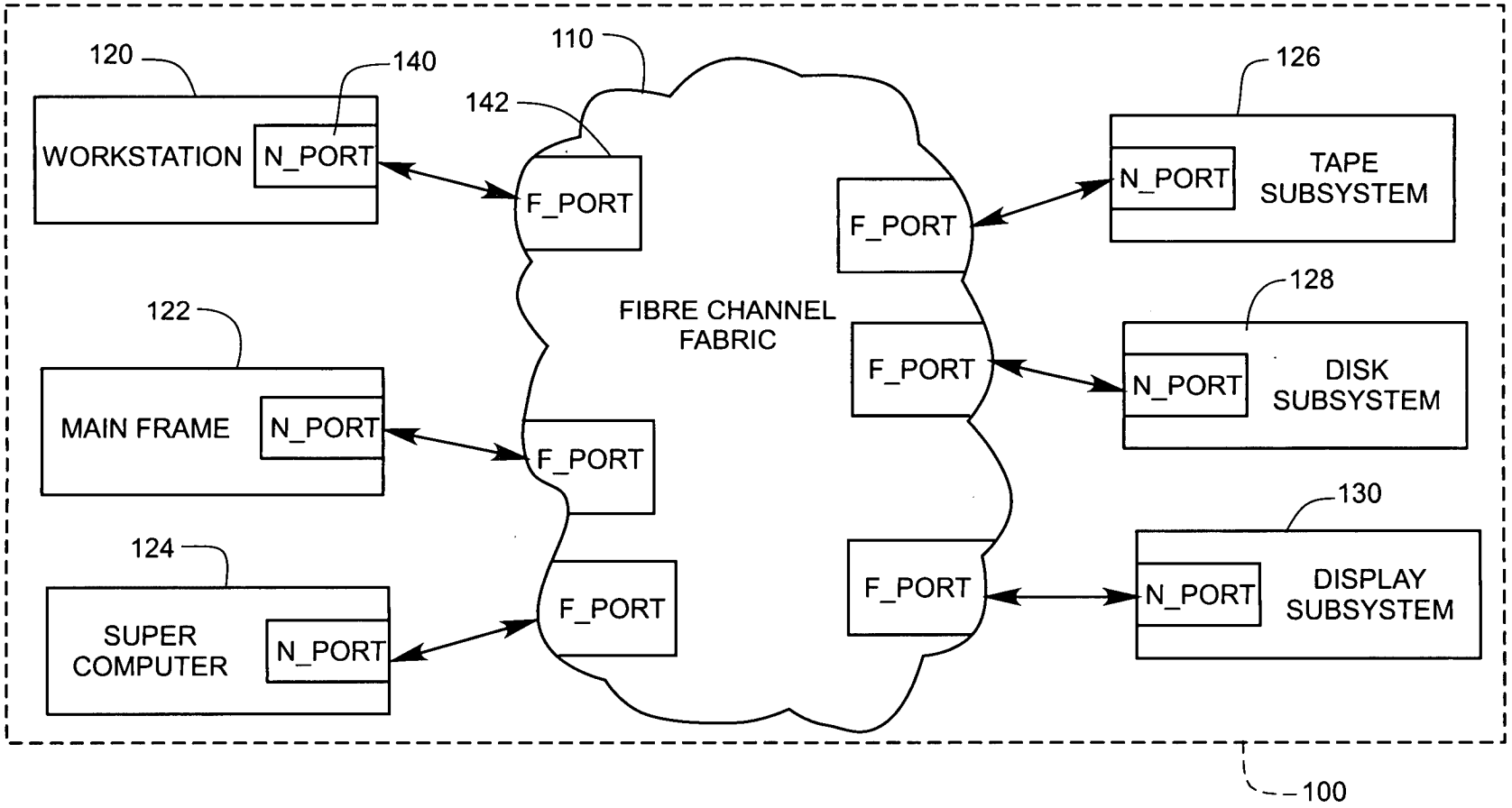


Fig. 3

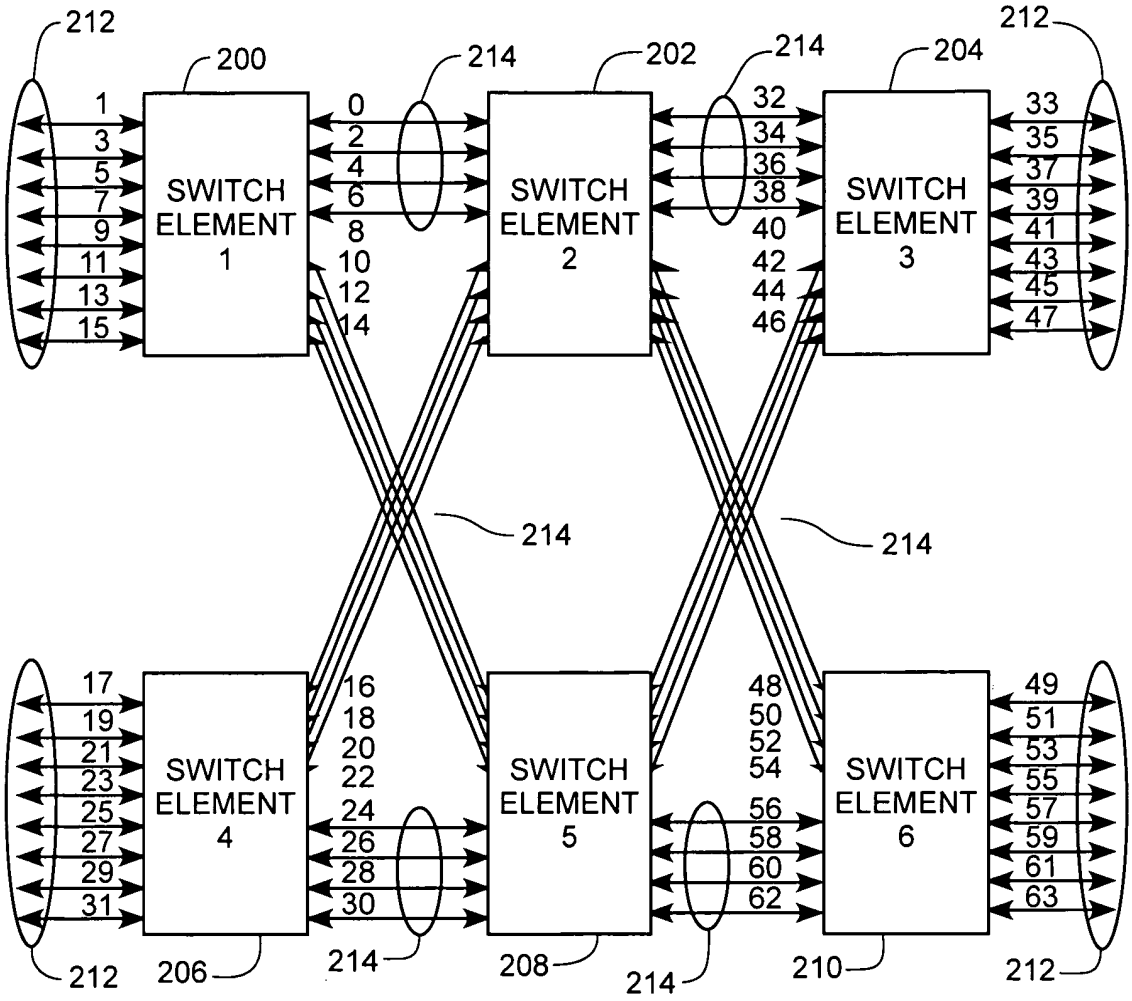

212
200
214
202
214
204
212
SWITCH ELEMENT 1
SWITCH ELEMENT 2
SWITCH ELEMENT 3
SWITCH ELEMENT 4
SWITCH ELEMENT 5
SWITCH ELEMENT 6
1
3
5
7
9
11
13
15
0
2
4
6
8
10
12
14
32
34
36
38
40
42
44
46
33
35
37
39
41
43
45
47
214
214
17
19
21
23
25
27
29
31
16
18
20
22
24
26
28
30
48
50
52
54
56
58
60
62
49
51
53
55
57
59
61
63
212
206
214
208
214
210
212

Fig. 4

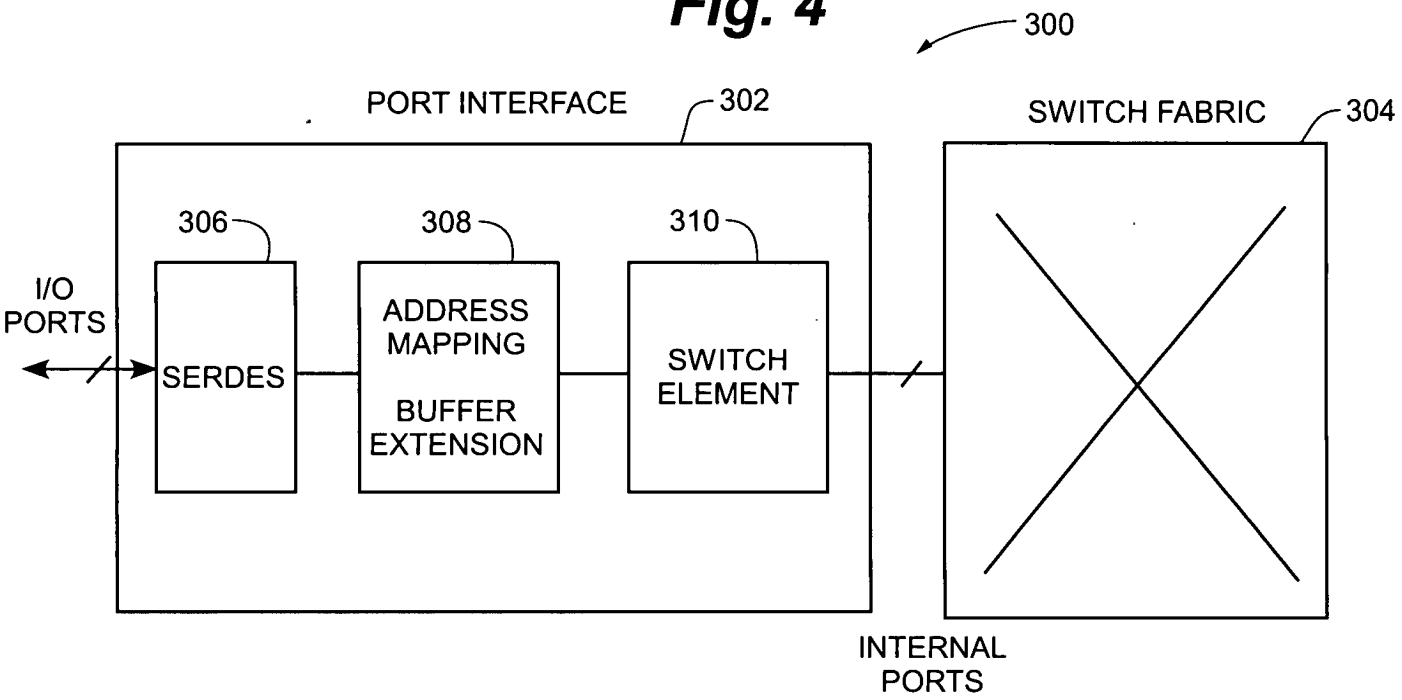

300
PORT INTERFACE
302
SWITCH FABRIC
304
306
308
310
I/O
PORTS
SERDES
ADDRESS
MAPPING
BUFFER
EXTENSION
SWITCH
ELEMENT
INTERNAL
PORTS

Fig. 5A

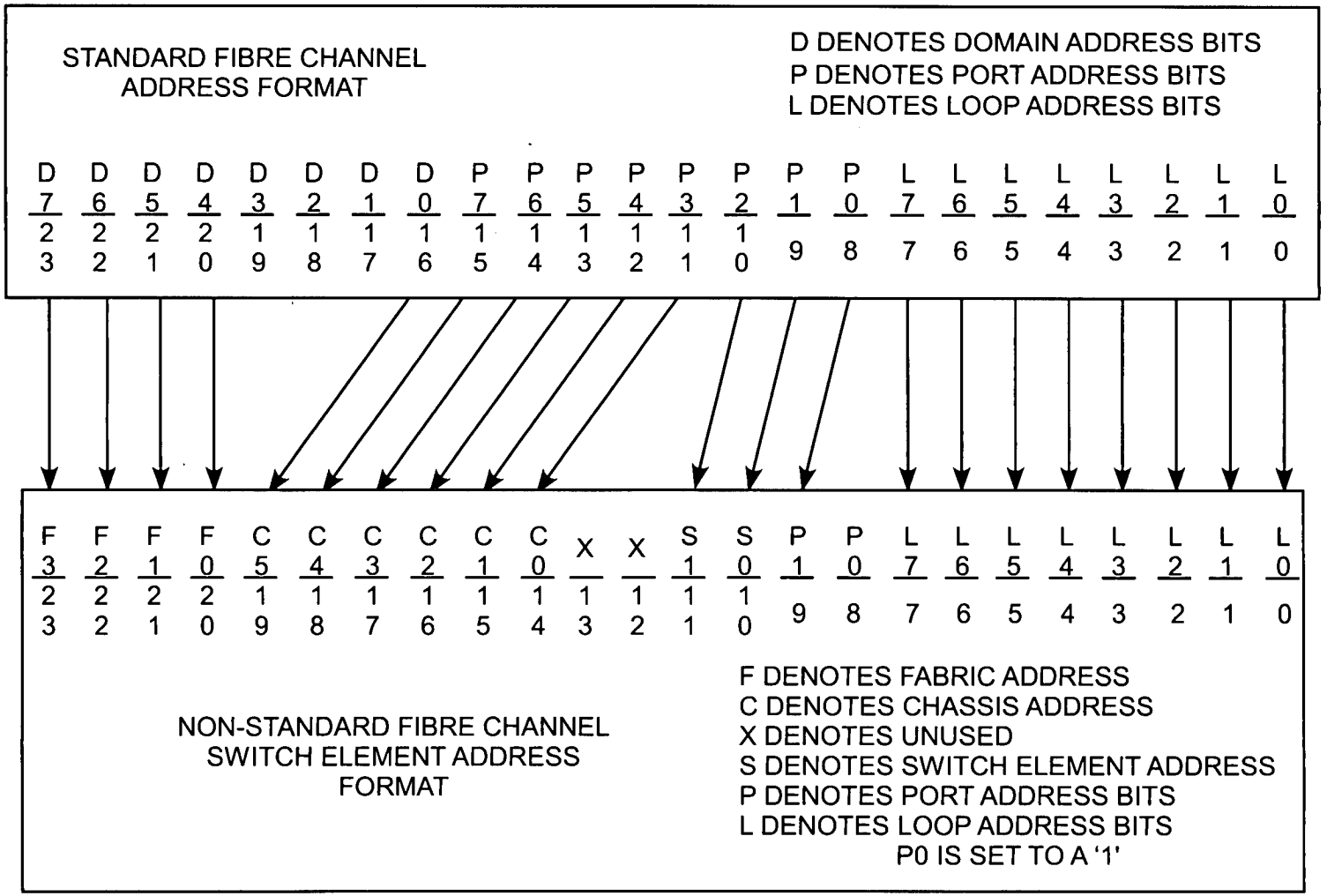

STANDARD FIBRE CHANNEL
ADDRESS FORMAT
D DENOTES DOMAIN ADDRESS BITS
P DENOTES PORT ADDRESS BITS
L DENOTES LOOP ADDRESS BITS
D7 D6 D5 D4 D3 D2 D1 D0 P7 P6 P5 P4 P3 P2 P1 P0 L7 L6 L5 L4 L3 L2 L1 L0
23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
F3 F2 F1 F0 C5 C4 C3 C2 C1 C0 X X S1 S0 P1 P0 L7 L6 L5 L4 L3 L2 L1 L0
23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
NON-STANDARD FIBRE CHANNEL
SWITCH ELEMENT ADDRESS
FORMAT
F DENOTES FABRIC ADDRESS
C DENOTES CHASSIS ADDRESS
X DENOTES UNUSED
S DENOTES SWITCH ELEMENT ADDRESS
P DENOTES PORT ADDRESS BITS
L DENOTES LOOP ADDRESS BITS
P0 IS SET TO A '1'

Fig. 5B

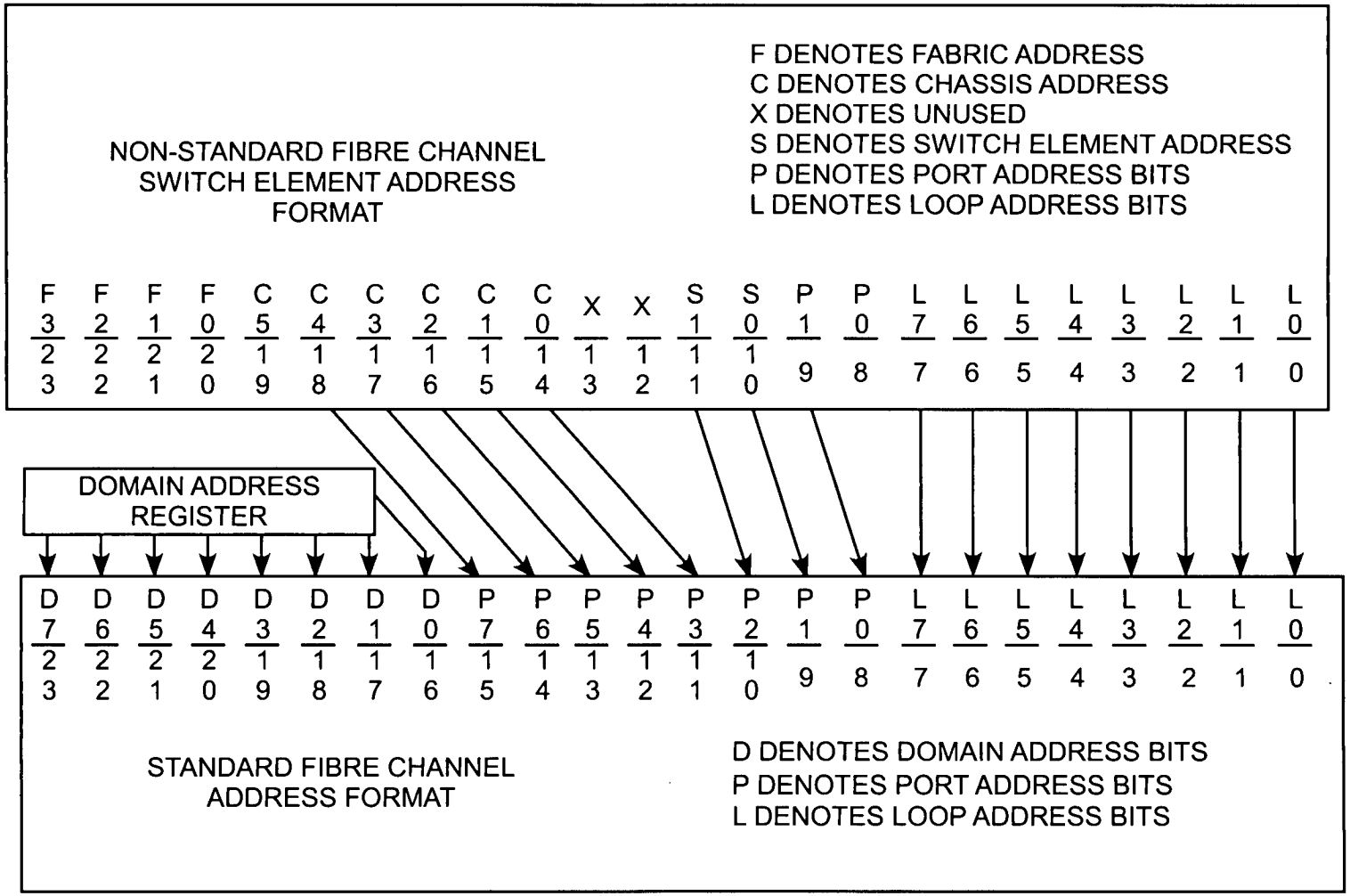

F DENOTES FABRIC ADDRESS
C DENOTES CHASSIS ADDRESS
X DENOTES UNUSED
S DENOTES SWITCH ELEMENT ADDRESS
P DENOTES PORT ADDRESS BITS
L DENOTES LOOP ADDRESS BITS
NON-STANDARD FIBRE CHANNEL SWITCH ELEMENT ADDRESS FORMAT
F32 F22 F12 F02 C519 C418 C317 C216 C115 C014 X13 X12 S11 S10 P1 P0 L7 L6 L5 L4 L3 L2 L1 L0
23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
DOMAIN ADDRESS REGISTER
D723 D622 D521 D420 D319 D218 D117 D016 P715 P614 P513 P412 P311 P210 P1 P0 L7 L6 L5 L4 L3 L2 L1 L0
23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
STANDARD FIBRE CHANNEL ADDRESS FORMAT
D DENOTES DOMAIN ADDRESS BITS
P DENOTES PORT ADDRESS BITS
L DENOTES LOOP ADDRESS BITS

Fig. 6

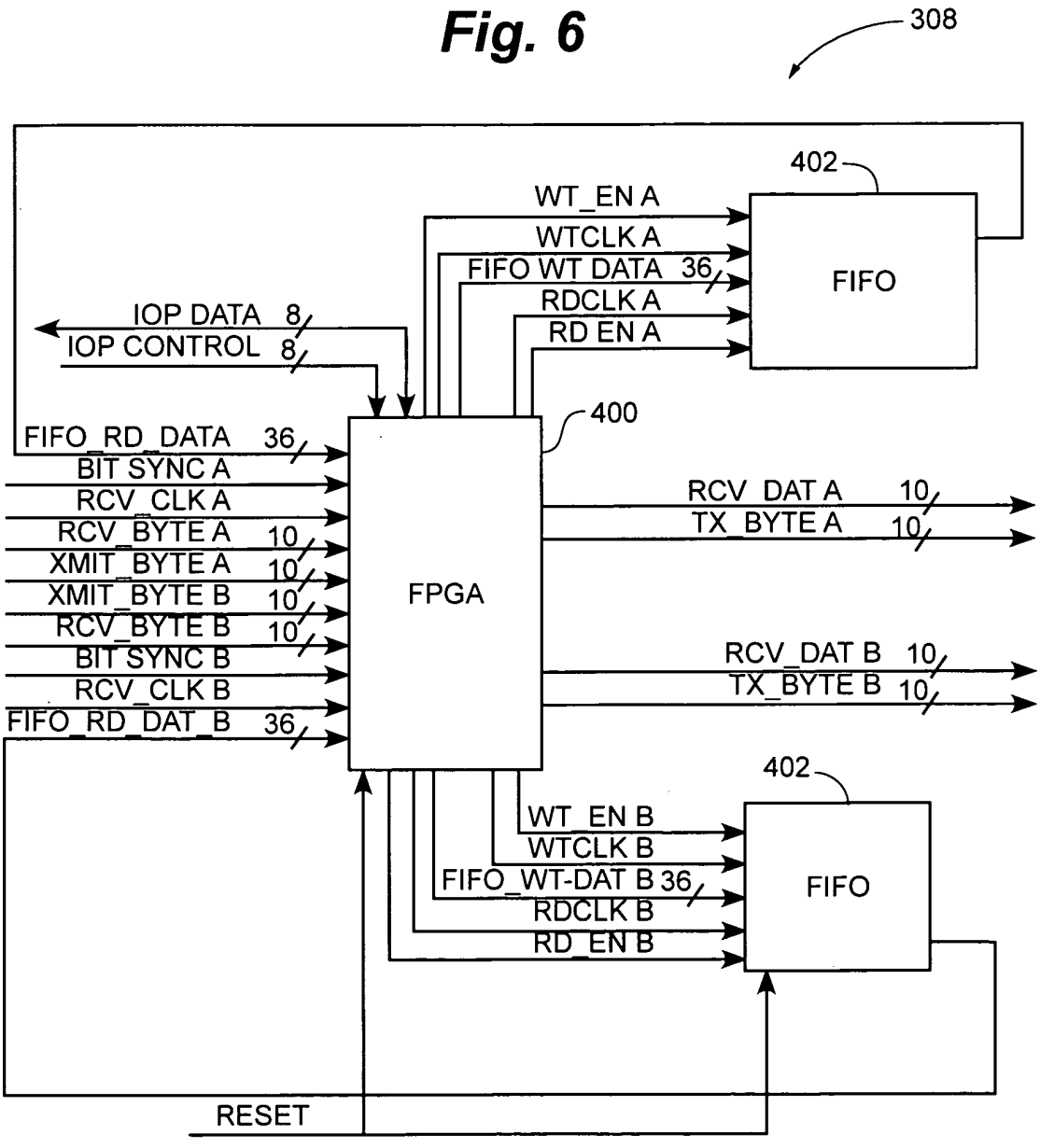

308
402
WT_EN A
WTCLK A
FIFO WT DATA 36
RDCLK A
RD EN A
FIFO
IOP DATA 8
IOP CONTROL 8
400
FIFO_RD_DATA 36
BIT SYNC A
RCV_CLK A
RCV_BYTE A 10
XMIT_BYTE A 10
XMIT_BYTE B 10
RCV_BYTE B 10
BIT SYNC B
RCV_CLK B
FIFO_RD_DAT_B 36
FPGA
RCV_DAT A 10
TX_BYTE A 10
RCV_DAT B 10
TX_BYTE B 10
402
WT_EN B
WTCLK B
FIFO_WT-DAT B 36
RDCLK B
RD_EN B
FIFO
RESET

Fig. 7

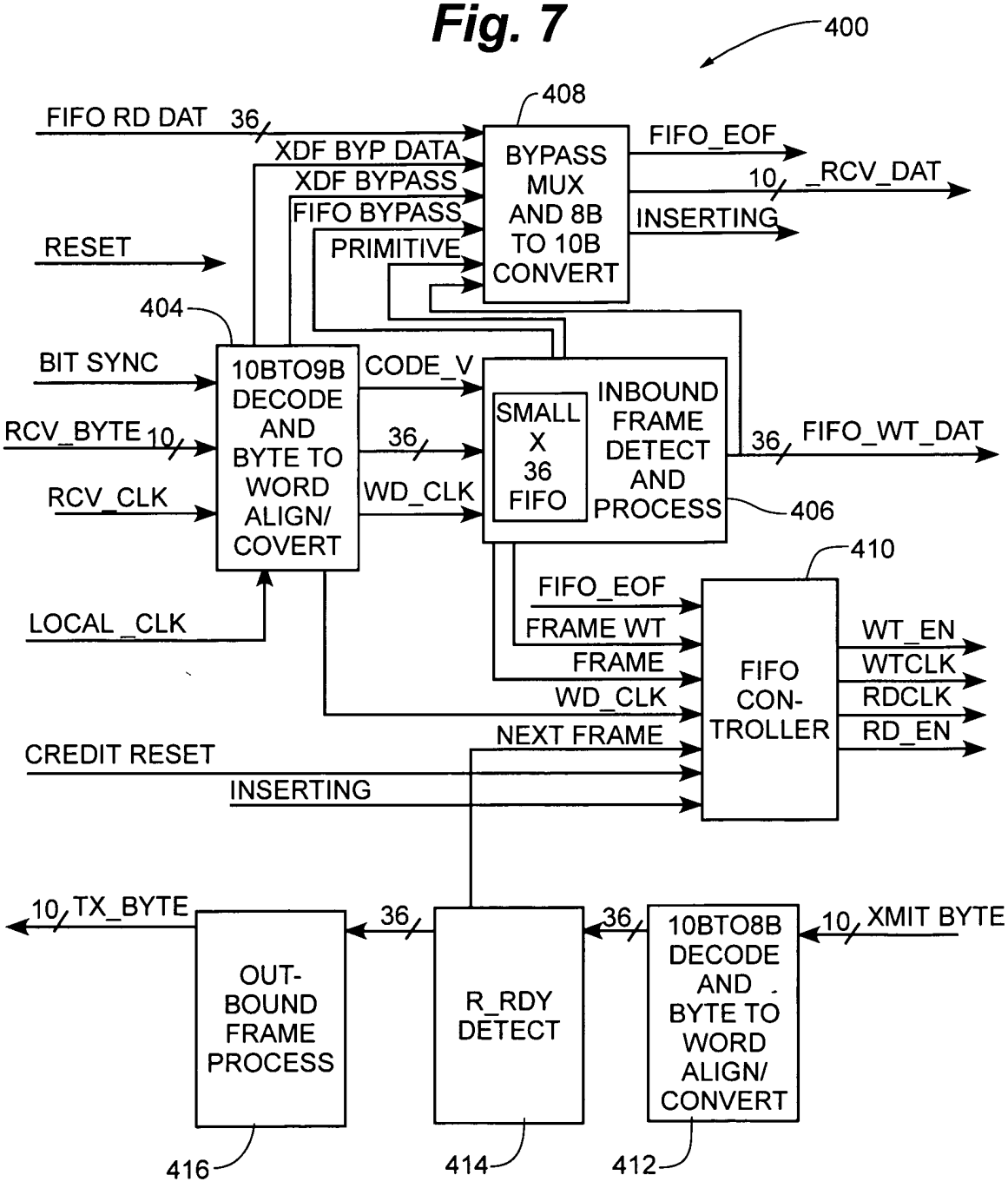

400
408
FIFO RD DAT
36
XDF BYP DATA
XDF BYPASS
FIFO BYPASS
PRIMITIVE
BYPASS MUX AND 8B TO 10B CONVERT
FIFO_EOF
10
_RCV_DAT
INSERTING
RESET
404
BIT SYNC
10BTO9B DECODE AND BYTE TO WORD ALIGN/ COVERT
CODE_V
RCV_BYTE
10
36
WD_CLK
RCV_CLK
SMALL X 36 FIFO
INBOUND FRAME DETECT AND PROCESS
36
FIFO_WT_DAT
406
410
LOCAL _CLK
FIFO_EOF
FRAME WT
FRAME
WD_CLK
NEXT FRAME
FIFO CON- TROLLER
WT_EN
WTCLK
RDCLK
RD_EN
CREDIT RESET
INSERTING
10
TX_BYTE
36
36
10
XMIT BYTE
OUT- BOUND FRAME PROCESS
R_RDY DETECT
10BTO8B DECODE AND BYTE TO WORD ALIGN/ CONVERT
416
414
412

Fig. 8

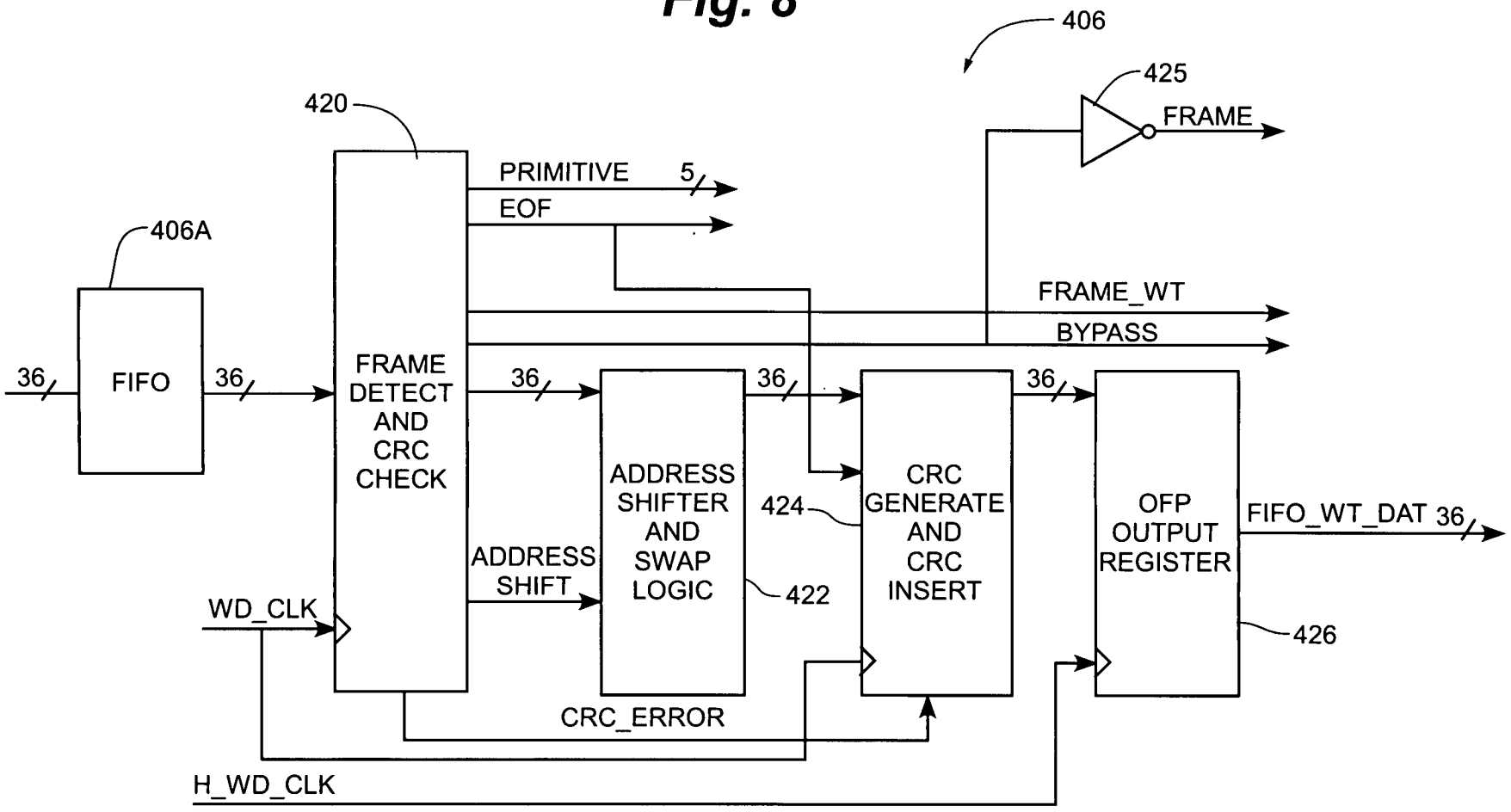

406
425
FRAME
420
PRIMITIVE
5
EOF
406A
FRAME_WT
BYPASS
36
FIFO
36
FRAME DETECT AND CRC CHECK
36
36
36
ADDRESS SHIFTER AND SWAP LOGIC
CRC GENERATE AND CRC INSERT
OFP OUTPUT REGISTER
FIFO_WT_DAT 36
424
ADDRESS SHIFT
422
WD_CLK
426
CRC_ERROR
H_WD_CLK

Fig. 9

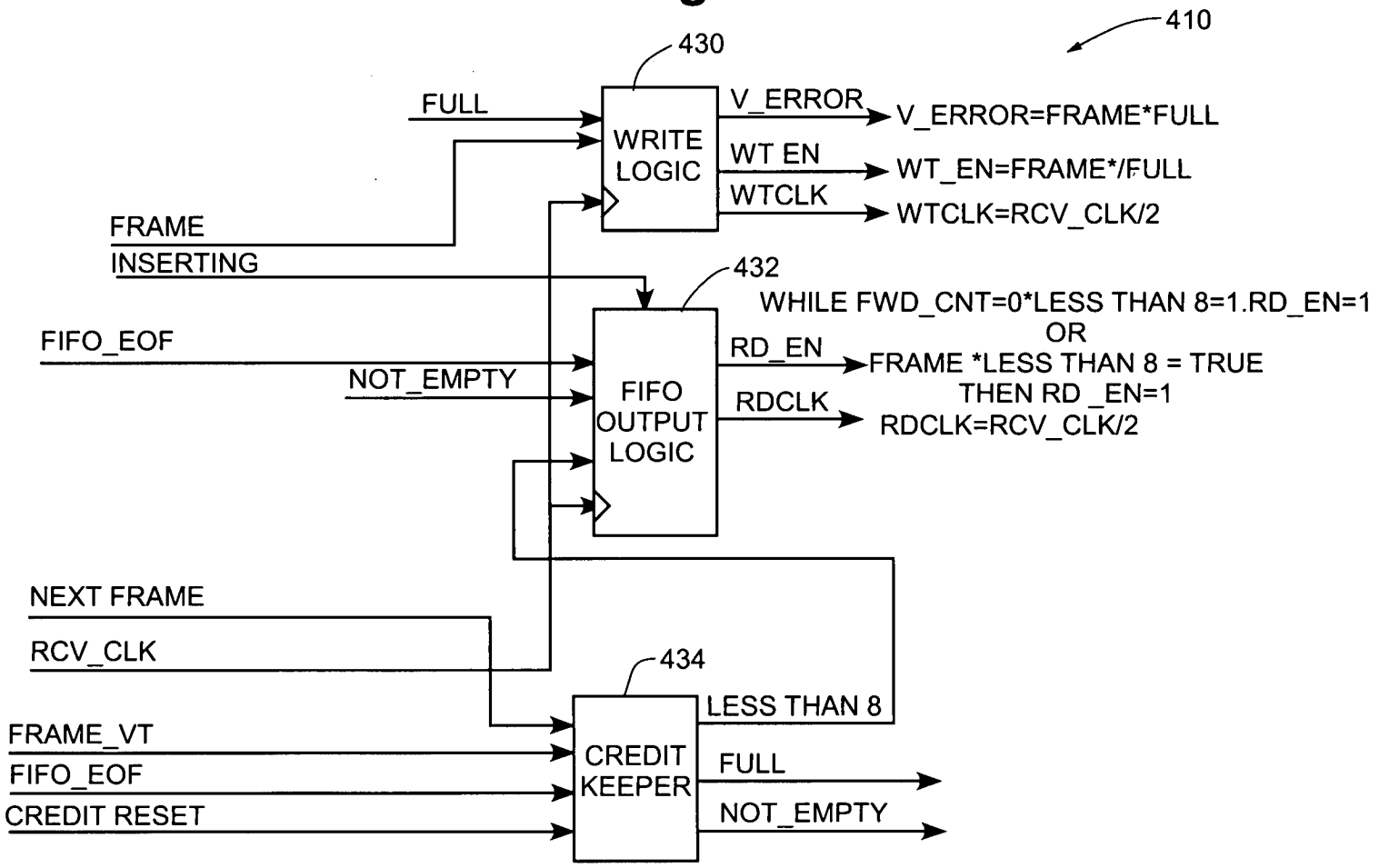

410
430
FULL
WRITE LOGIC
V_ERROR
V_ERROR=FRAME*FULL
WT EN
WT_EN=FRAME*/FULL
WTCLK
WTCLK=RCV_CLK/2
FRAME
INSERTING
432
WHILE FWD_CNT=0*LESS THAN 8=1.RD_EN=1
OR
FRAME *LESS THAN 8 = TRUE
THEN RD _EN=1
FIFO_EOF
NOT_EMPTY
FIFO OUTPUT LOGIC
RD_EN
RDCLK
RDCLK=RCV_CLK/2
NEXT FRAME
RCV_CLK
434
LESS THAN 8
FRAME_VT
FIFO_EOF
CREDIT RESET
CREDIT KEEPER
FULL
NOT_EMPTY

Fig. 10

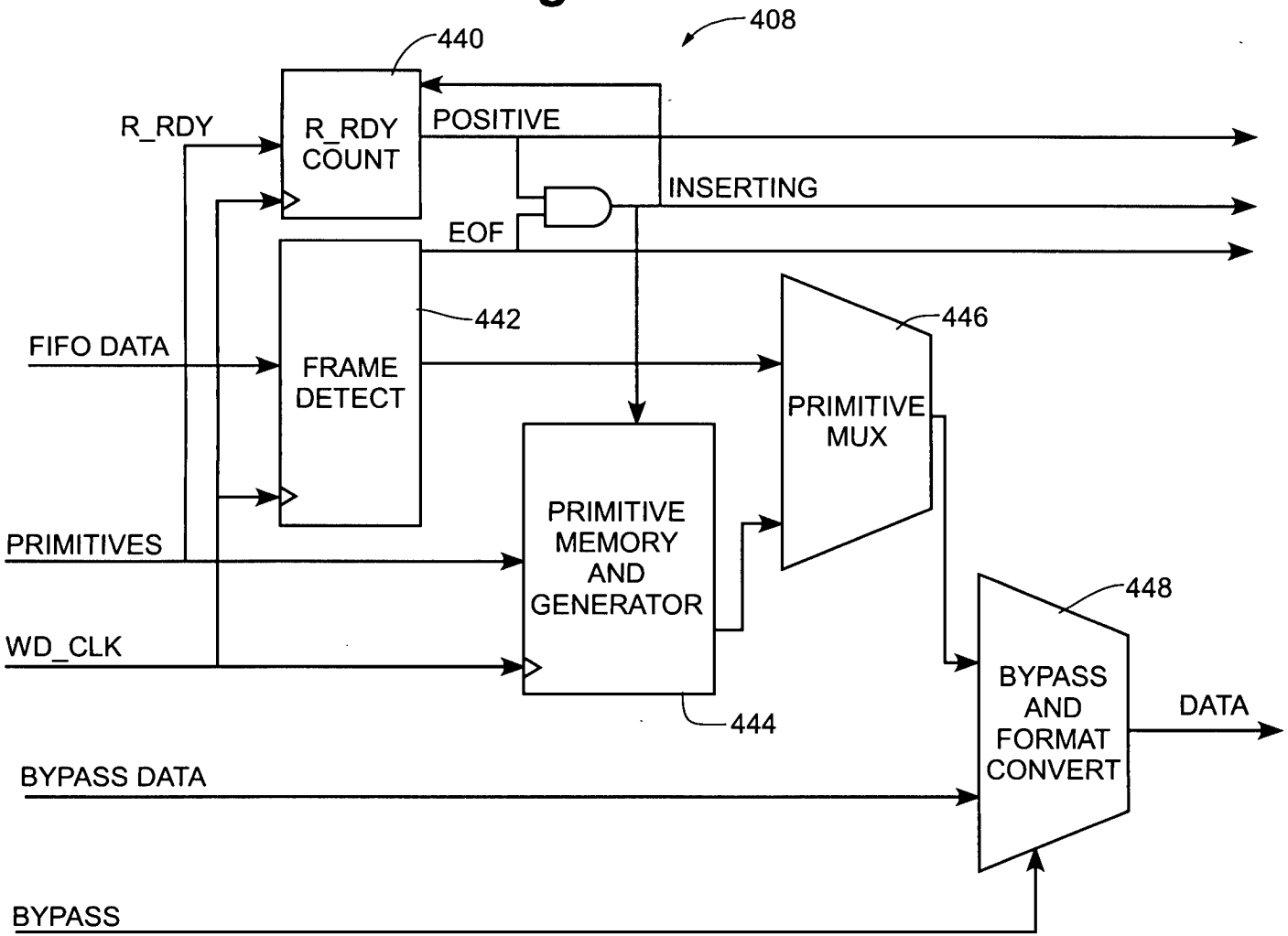

408
440
R_RDY
R_RDY COUNT
POSITIVE
INSERTING
EOF
442
FIFO DATA
FRAME DETECT
446
PRIMITIVE MUX
PRIMITIVE MEMORY AND GENERATOR
PRIMITIVES
WD_CLK
444
448
BYPASS AND FORMAT CONVERT
DATA
BYPASS DATA
BYPASS

Fig. 11

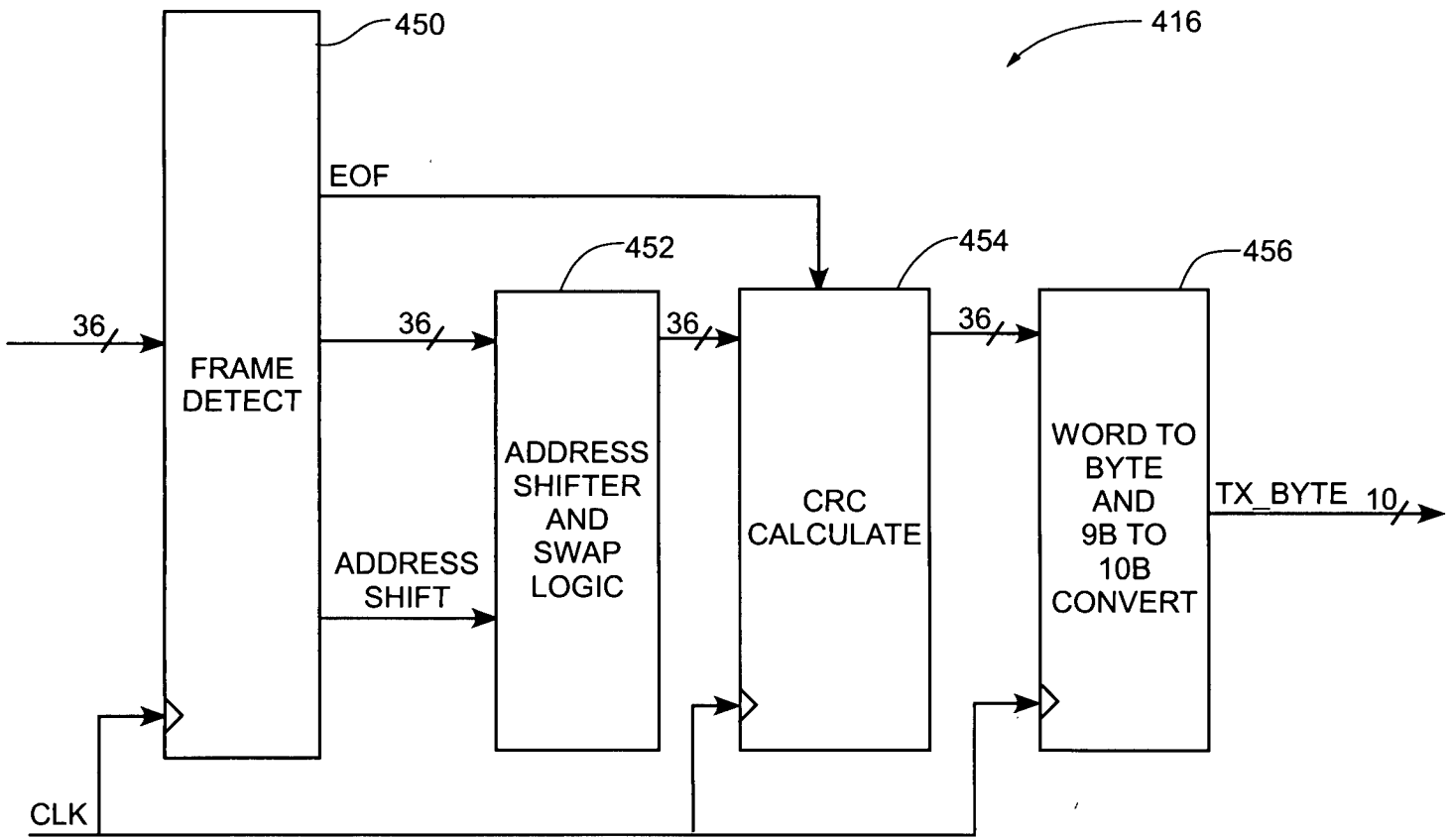

450
416
EOF
452
454
456
36
36
36
36
FRAME DETECT
ADDRESS SHIFTER AND SWAP LOGIC
CRC CALCULATE
WORD TO BYTE AND 9B TO 10B CONVERT
TX_BYTE
10
ADDRESS SHIFT
CLK

Fig. 12

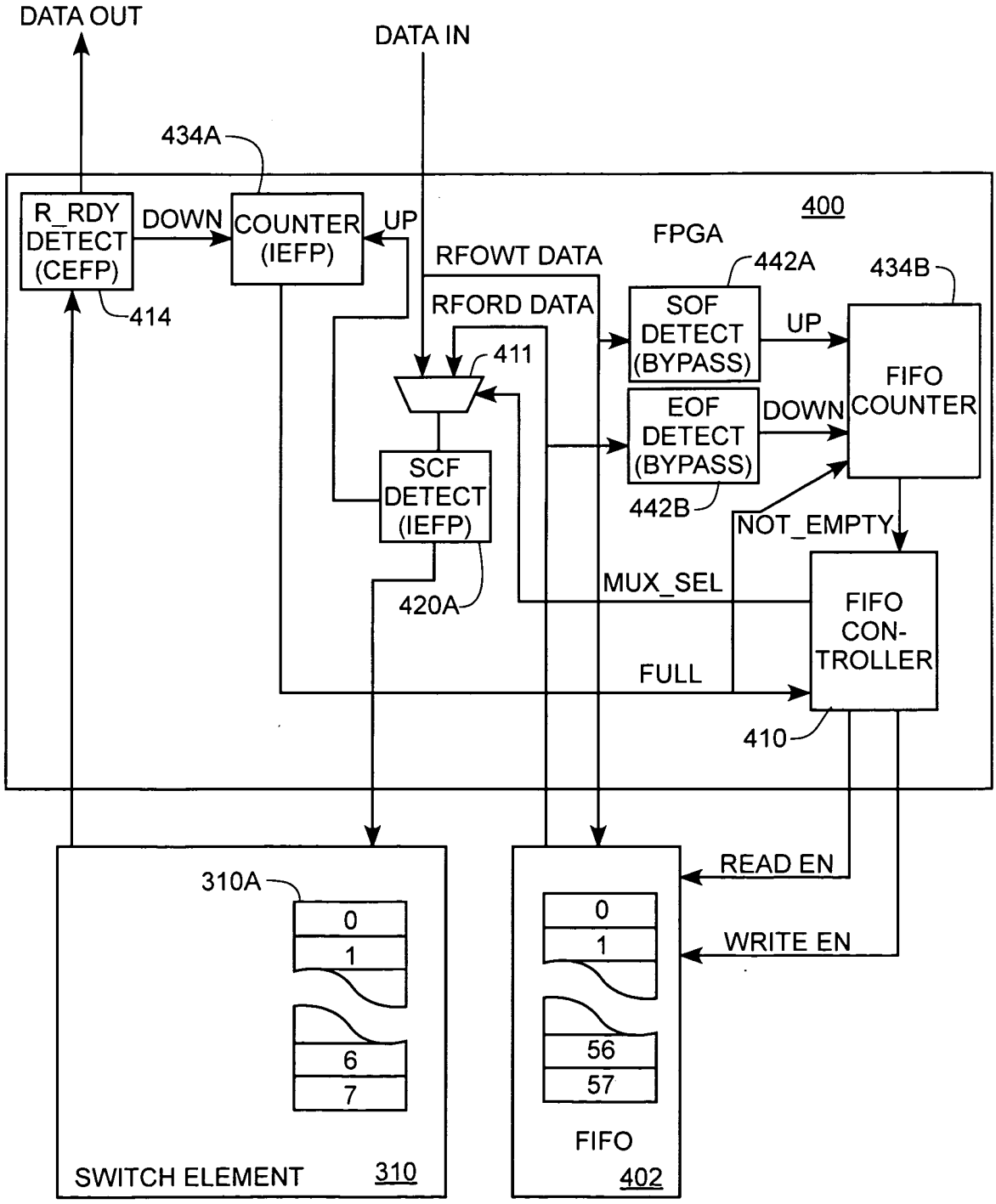

DATA OUT
DATA IN
434A
400
R_RDY DETECT (CEFP)
DOWN
COUNTER (IEFP)
UP
414
FPGA
RFOWT DATA
RFORD DATA
442A
434B
SOF DETECT (BYPASS)
UP
FIFO COUNTER
411
EOF DETECT (BYPASS)
DOWN
SCF DETECT (IEFP)
442B
NOT_EMPTY
MUX_SEL
FIFO CON-TROLLER
420A
FULL
410
READ EN
310A
0
1
6
7
SWITCH ELEMENT
310
0
1
56
57
WRITE EN
FIFO
402

Fig. 13

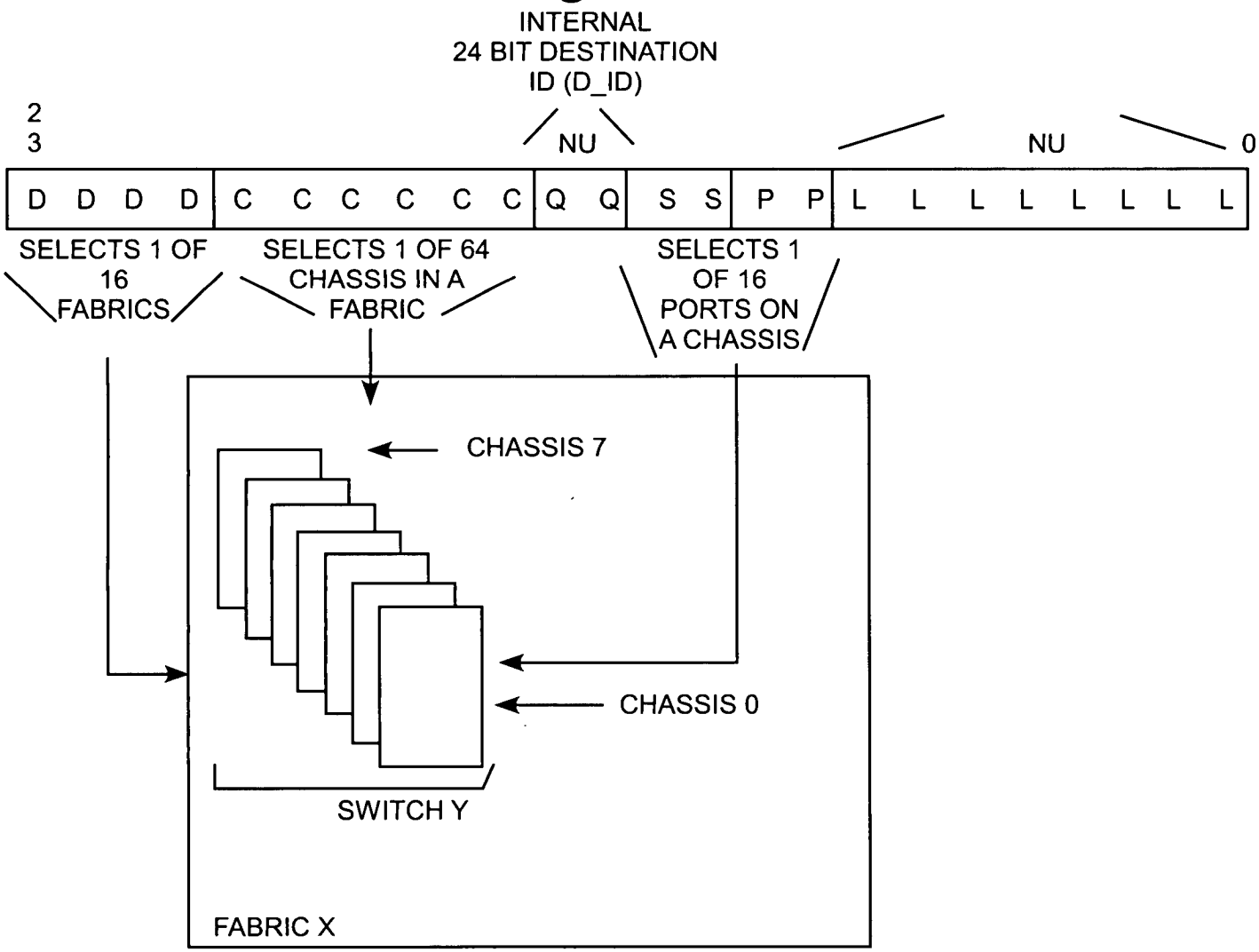

INTERNAL
24 BIT DESTINATION
ID (D_ID)
2
3
NU
NU
0
D D D D
C C C C C C
Q Q
S S
P P
L L L L L L L L
SELECTS 1 OF
16
FABRICS
SELECTS 1 OF 64
CHASSIS IN A
FABRIC
SELECTS 1
OF 16
PORTS ON
A CHASSIS
CHASSIS 7
CHASSIS 0
SWITCH Y
FABRIC X

Fig. 14

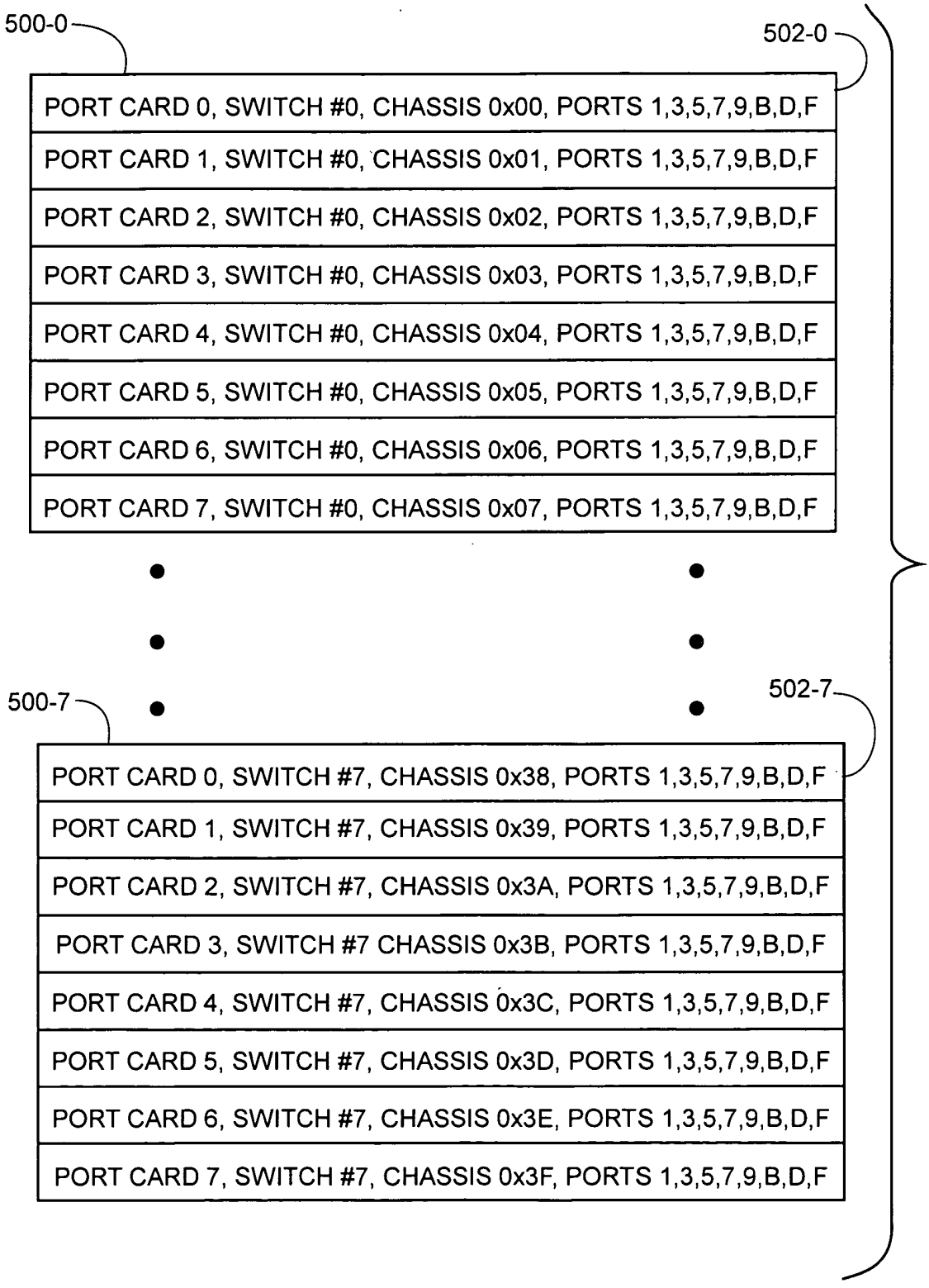

500-0
502-0
PORT CARD 0, SWITCH #0, CHASSIS 0x00, PORTS 1,3,5,7,9,B,D,F
PORT CARD 1, SWITCH #0, CHASSIS 0x01, PORTS 1,3,5,7,9,B,D,F
PORT CARD 2, SWITCH #0, CHASSIS 0x02, PORTS 1,3,5,7,9,B,D,F
PORT CARD 3, SWITCH #0, CHASSIS 0x03, PORTS 1,3,5,7,9,B,D,F
PORT CARD 4, SWITCH #0, CHASSIS 0x04, PORTS 1,3,5,7,9,B,D,F
PORT CARD 5, SWITCH #0, CHASSIS 0x05, PORTS 1,3,5,7,9,B,D,F
PORT CARD 6, SWITCH #0, CHASSIS 0x06, PORTS 1,3,5,7,9,B,D,F
PORT CARD 7, SWITCH #0, CHASSIS 0x07, PORTS 1,3,5,7,9,B,D,F
500-7
502-7
PORT CARD 0, SWITCH #7, CHASSIS 0x38, PORTS 1,3,5,7,9,B,D,F
PORT CARD 1, SWITCH #7, CHASSIS 0x39, PORTS 1,3,5,7,9,B,D,F
PORT CARD 2, SWITCH #7, CHASSIS 0x3A, PORTS 1,3,5,7,9,B,D,F
PORT CARD 3, SWITCH #7 CHASSIS 0x3B, PORTS 1,3,5,7,9,B,D,F
PORT CARD 4, SWITCH #7, CHASSIS 0x3C, PORTS 1,3,5,7,9,B,D,F
PORT CARD 5, SWITCH #7, CHASSIS 0x3D, PORTS 1,3,5,7,9,B,D,F
PORT CARD 6, SWITCH #7, CHASSIS 0x3E, PORTS 1,3,5,7,9,B,D,F
PORT CARD 7, SWITCH #7, CHASSIS 0x3F, PORTS 1,3,5,7,9,B,D,F

Fig. 15

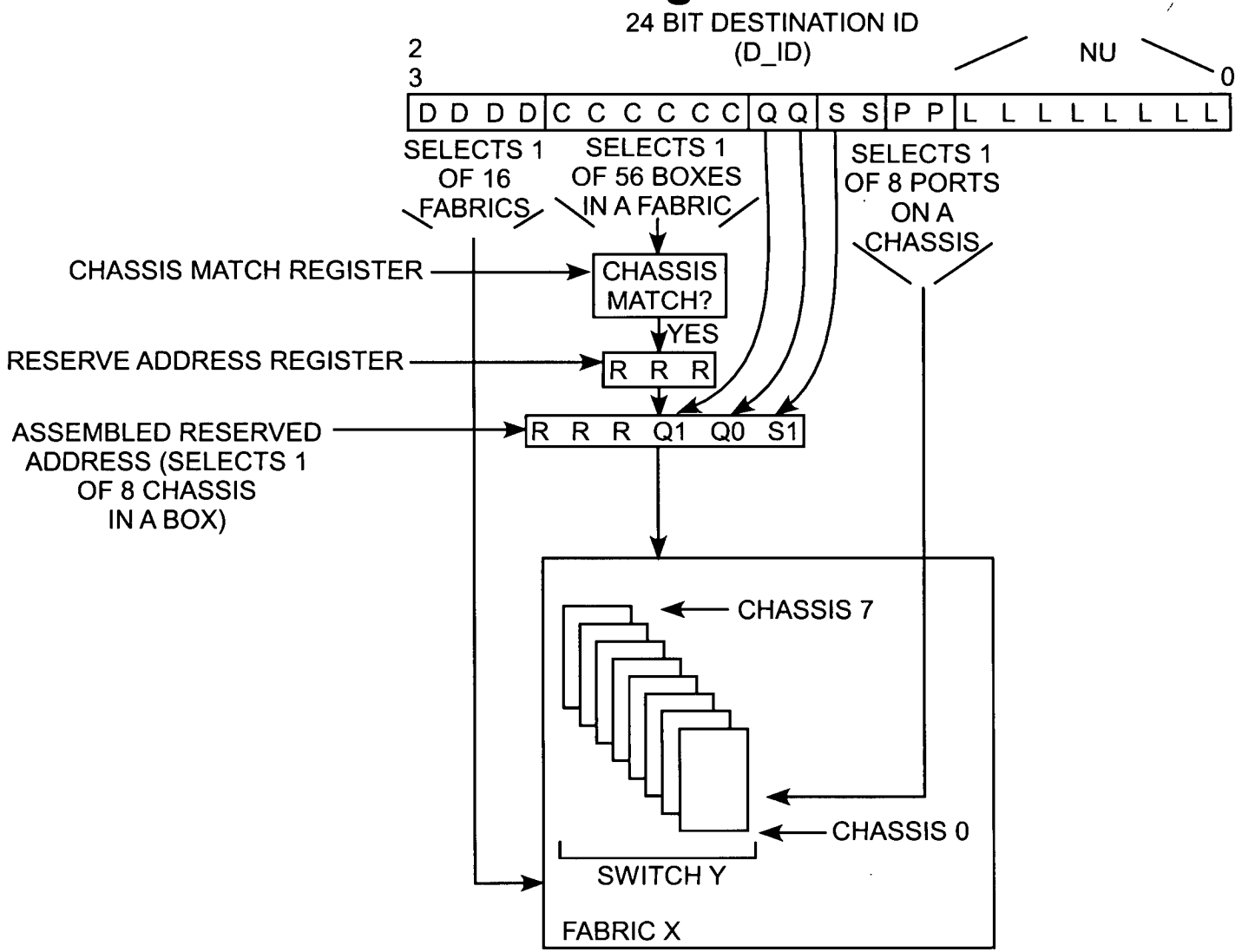

24 BIT DESTINATION ID
(D_ID)
2
3
NU
0
D D D D C C C C C C Q Q S S P P L L L L L L L L
SELECTS 1 OF 16 FABRICS
SELECTS 1 OF 56 BOXES IN A FABRIC
SELECTS 1 OF 8 PORTS ON A CHASSIS
CHASSIS MATCH REGISTER
CHASSIS MATCH?
YES
RESERVE ADDRESS REGISTER
R R R
ASSEMBLED RESERVED ADDRESS (SELECTS 1 OF 8 CHASSIS IN A BOX)
R R R Q1 Q0 S1
CHASSIS 7
CHASSIS 0
SWITCH Y
FABRIC X

Fig. 16

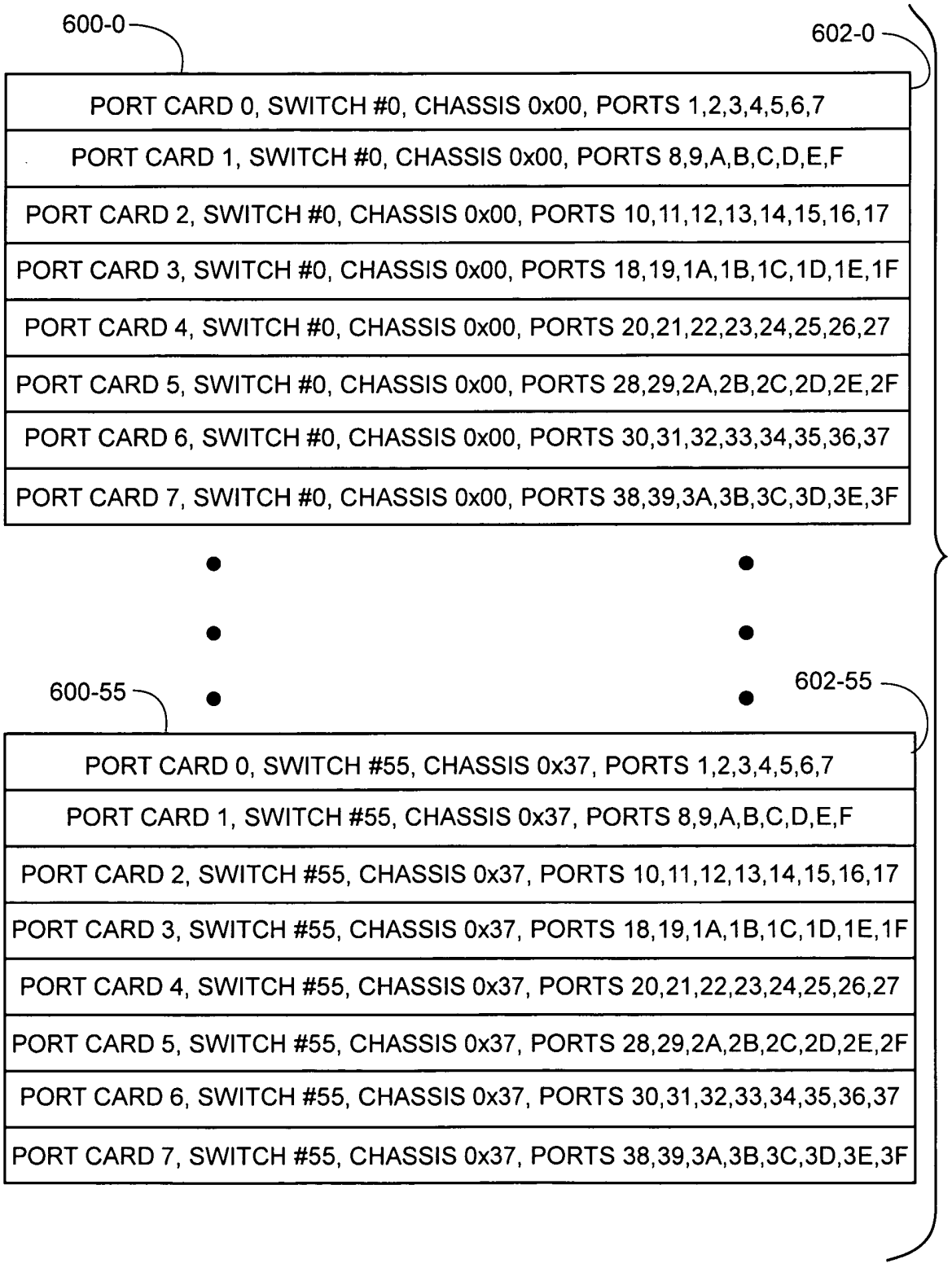

600-0
602-0
PORT CARD 0, SWITCH #0, CHASSIS 0x00, PORTS 1,2,3,4,5,6,7
PORT CARD 1, SWITCH #0, CHASSIS 0x00, PORTS 8,9,A,B,C,D,E,F
PORT CARD 2, SWITCH #0, CHASSIS 0x00, PORTS 10,11,12,13,14,15,16,17
PORT CARD 3, SWITCH #0, CHASSIS 0x00, PORTS 18,19,1A,1B,1C,1D,1E,1F
PORT CARD 4, SWITCH #0, CHASSIS 0x00, PORTS 20,21,22,23,24,25,26,27
PORT CARD 5, SWITCH #0, CHASSIS 0x00, PORTS 28,29,2A,2B,2C,2D,2E,2F
PORT CARD 6, SWITCH #0, CHASSIS 0x00, PORTS 30,31,32,33,34,35,36,37
PORT CARD 7, SWITCH #0, CHASSIS 0x00, PORTS 38,39,3A,3B,3C,3D,3E,3F
600-55
602-55
PORT CARD 0, SWITCH #55, CHASSIS 0x37, PORTS 1,2,3,4,5,6,7
PORT CARD 1, SWITCH #55, CHASSIS 0x37, PORTS 8,9,A,B,C,D,E,F
PORT CARD 2, SWITCH #55, CHASSIS 0x37, PORTS 10,11,12,13,14,15,16,17
PORT CARD 3, SWITCH #55, CHASSIS 0x37, PORTS 18,19,1A,1B,1C,1D,1E,1F
PORT CARD 4, SWITCH #55, CHASSIS 0x37, PORTS 20,21,22,23,24,25,26,27
PORT CARD 5, SWITCH #55, CHASSIS 0x37, PORTS 28,29,2A,2B,2C,2D,2E,2F
PORT CARD 6, SWITCH #55, CHASSIS 0x37, PORTS 30,31,32,33,34,35,36,37
PORT CARD 7, SWITCH #55, CHASSIS 0x37, PORTS 38,39,3A,3B,3C,3D,3E,3F

Fig. 17

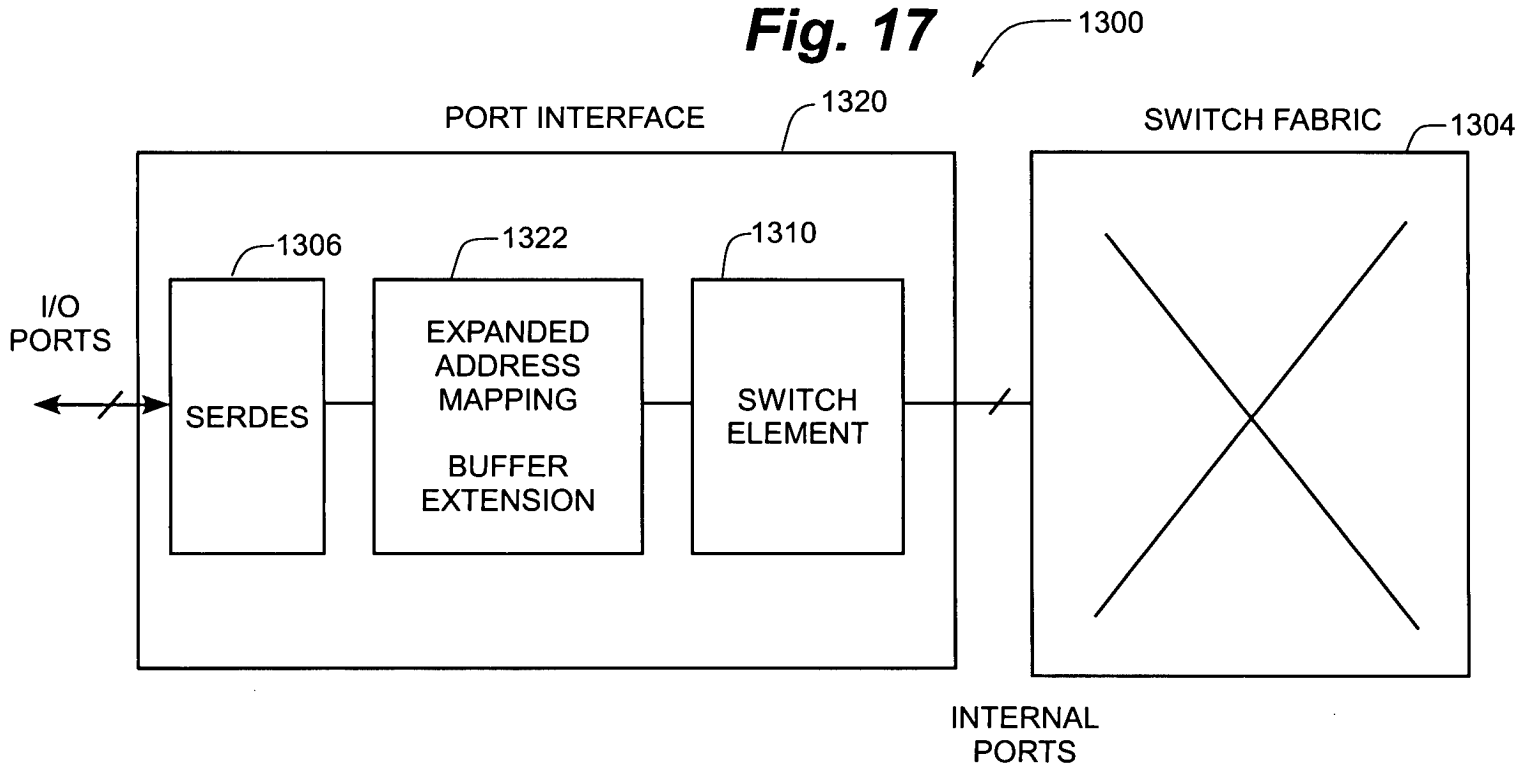

1300
PORT INTERFACE
1320
SWITCH FABRIC
1304
1306
1322
1310
I/O
PORTS
SERDES
EXPANDED
ADDRESS
MAPPING
BUFFER
EXTENSION
SWITCH
ELEMENT
INTERNAL
PORTS

Fig. 18

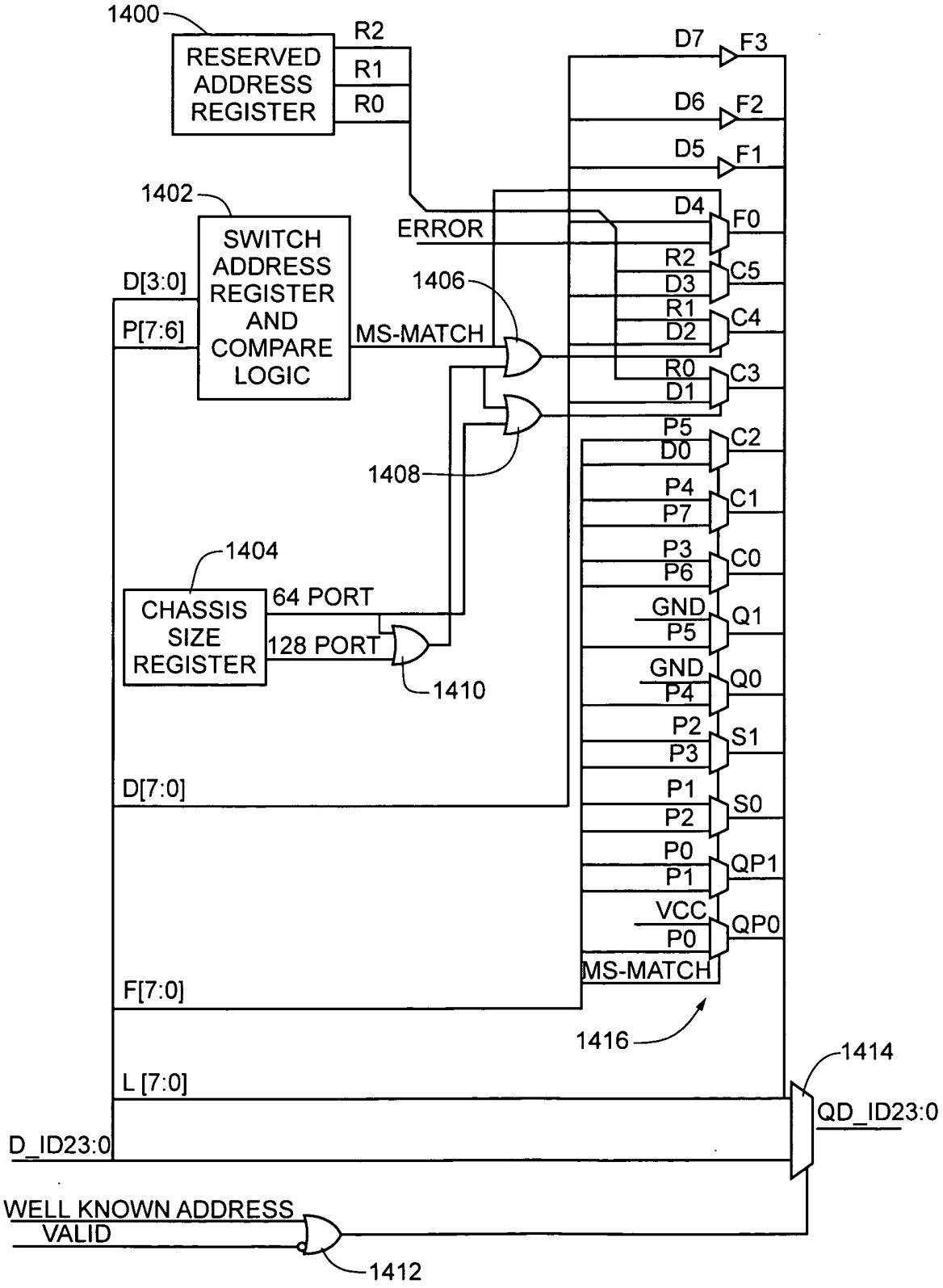

1400
RESERVED ADDRESS REGISTER
R2
R1
R0
1402
SWITCH ADDRESS REGISTER AND COMPARE LOGIC
D[3:0]
P[7:6]
ERROR
MS-MATCH
1406
1408
1404
CHASSIS SIZE REGISTER
64 PORT
128 PORT
1410
D[7:0]
F[7:0]
L [7:0]
D_ID23:0
WELL KNOWN ADDRESS VALID
1412
D7
F3
D6
F2
D5
F1
D4
F0
R2
D3
C5
R1
D2
C4
R0
D1
C3
P5
D0
C2
P4
P7
C1
P3
P6
C0
GND
P5
Q1
GND
P4
Q0
P2
P3
S1
P1
P2
S0
P0
P1
QP1
VCC
P0
QP0
MS-MATCH
1416
1414
QD_ID23:0

Fig. 19

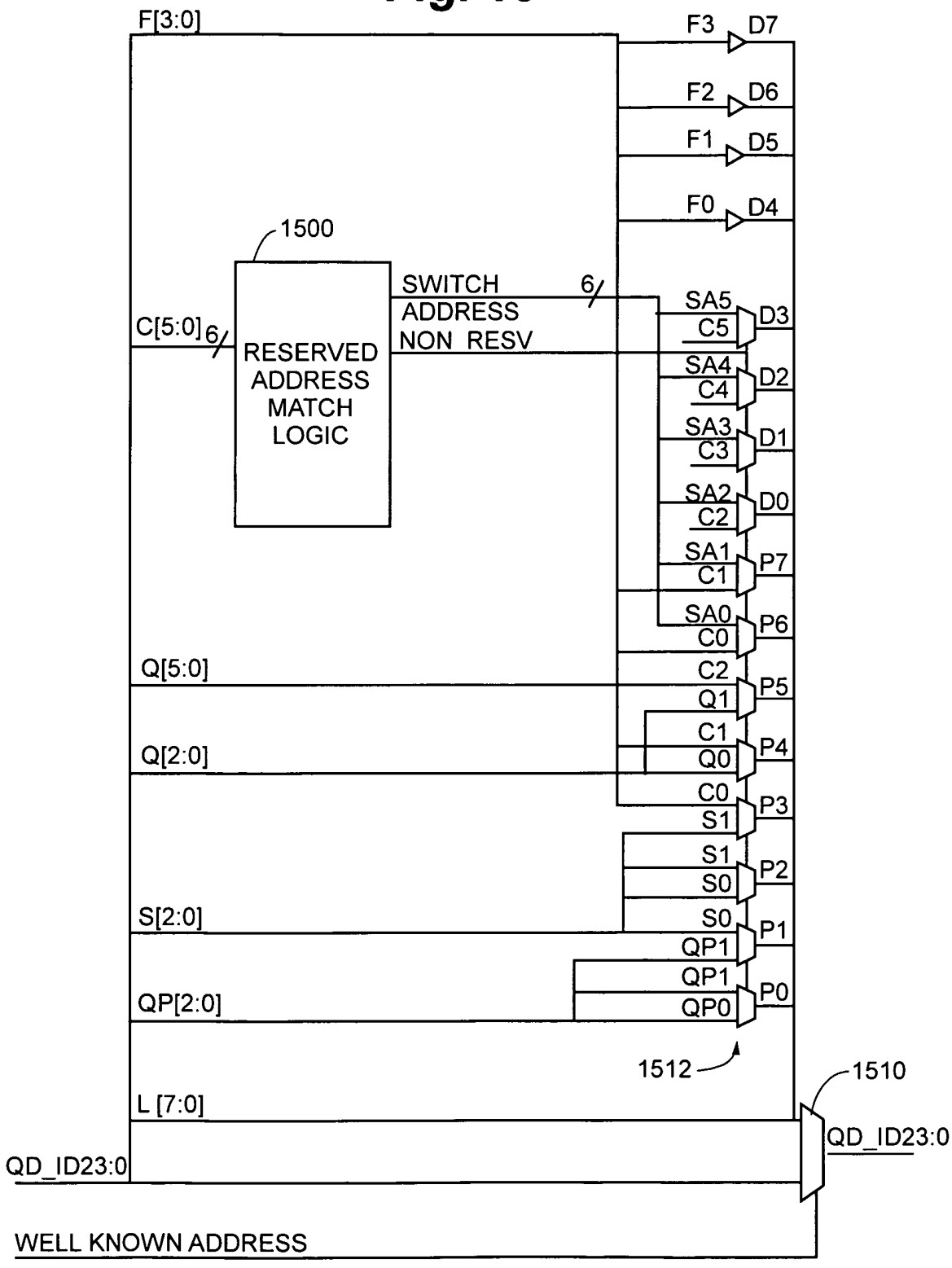

F[3:0]
F3
D7
F2
D6
F1
D5
F0
D4
1500
SWITCH
ADDRESS
NON RESV
6
C[5:0]
6
RESERVED
ADDRESS
MATCH
LOGIC
SA5
C5
D3
SA4
C4
D2
SA3
C3
D1
SA2
C2
D0
SA1
C1
P7
SA0
C0
P6
Q[5:0]
C2
Q1
P5
C1
Q0
P4
Q[2:0]
C0
S1
P3
S1
S0
P2
S[2:0]
S0
QP1
P1
QP1
QP0
P0
QP[2:0]
1512
1510
L [7:0]
QD_ID23:0
QD_ID23:0
WELL KNOWN ADDRESS

Fig. 20

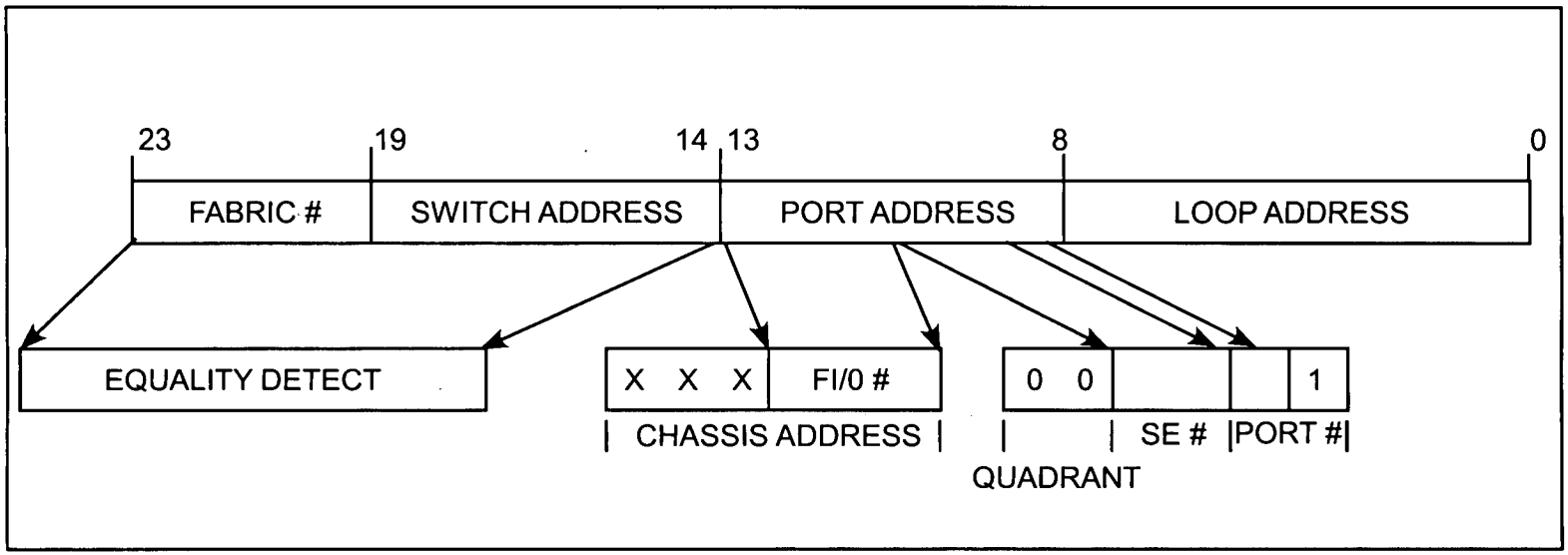

23
19
14
13
8
0
FABRIC #
SWITCH ADDRESS
PORT ADDRESS
LOOP ADDRESS
EQUALITY DETECT
X X X
FI/0 #
CHASSIS ADDRESS
0 0
1
QUADRANT
SE #
PORT #

Fig. 21

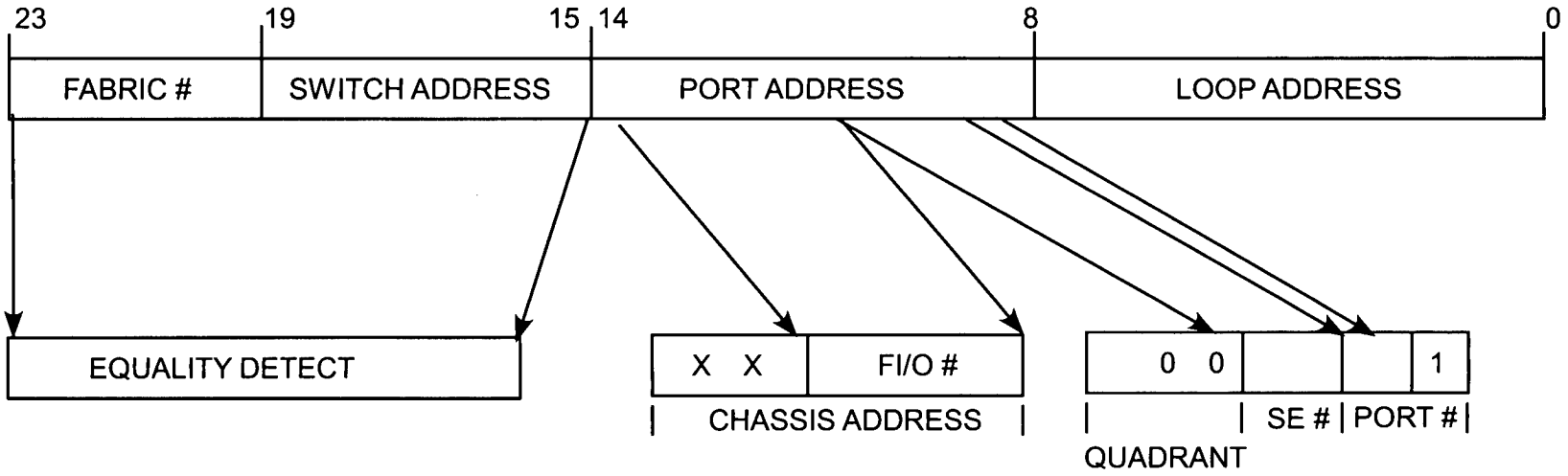

23
19
15
14
8
0
FABRIC #
SWITCH ADDRESS
PORT ADDRESS
LOOP ADDRESS
EQUALITY DETECT
X X
FI/O #
CHASSIS ADDRESS
0 0
1
SE #
PORT #
QUADRANT

Fig. 22

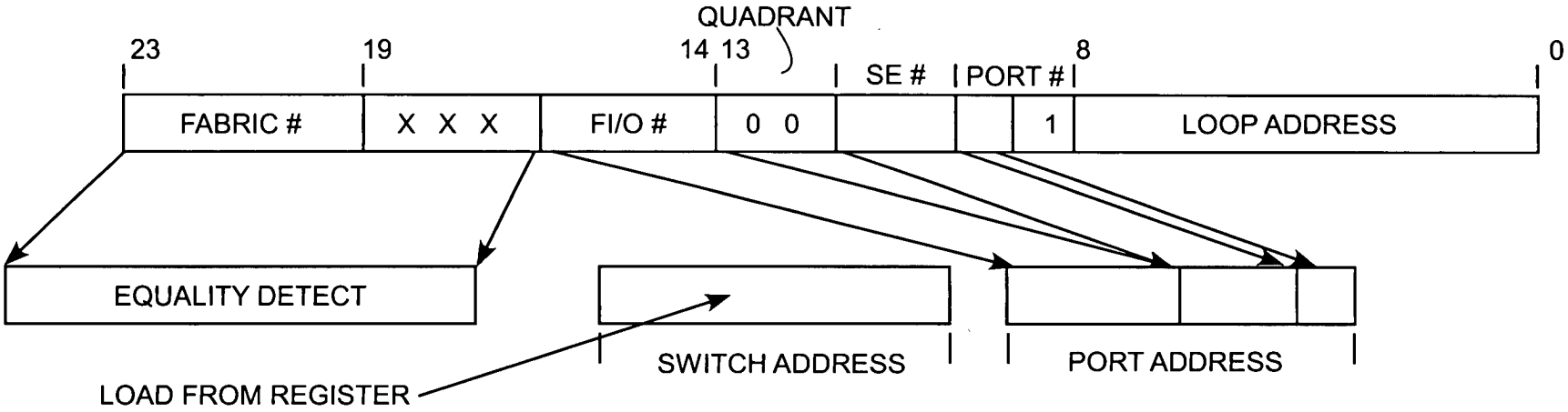
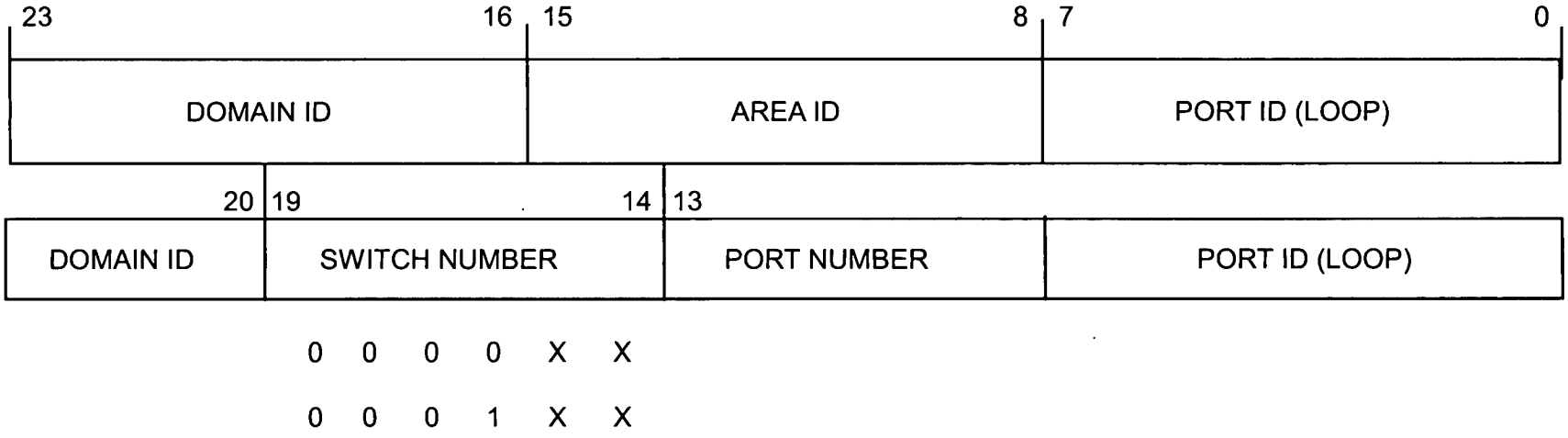

QUADRANT
23
19
14 13
8
0
SE #
PORT #
FABRIC #
X X X
FI/O #
0 0
1
LOOP ADDRESS
EQUALITY DETECT
SWITCH ADDRESS
PORT ADDRESS
LOAD FROM REGISTER

Fig. 23


23
16
15
8
7
0
DOMAIN ID
AREA ID
PORT ID (LOOP)
20
19
14
13
DOMAIN ID
SWITCH NUMBER
PORT NUMBER
PORT ID (LOOP)
0 0 0 0 X X
0 0 0 1 X X